

REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION Unclassified		1b. RESTRICTIVE MARKINGS	
AD-A202 023		3 DISTRIBUTION / AVAILABILITY OF REPORT Approved for public release; distribution unlimited.	
4 PERFORMING ORGANIZATION REPORT NUMBER(S)		5. MONITORING ORGANIZATION REPORT NUMBER(S) ARO 25601.2-EL	
6a. NAME OF PERFORMING ORGANIZATION North Carolina State Univ	6b. OFFICE SYMBOL (If applicable)	7a. NAME OF MONITORING ORGANIZATION U. S. Army Research Office	
6c. ADDRESS (City, State, and ZIP Code) Dept. of Electrical & Computer Engineering Raleigh, N.C. 27695-7911		7b. ADDRESS (City, State, and ZIP Code) P. O. Box 12211 Research Triangle Park, NC 27709-2211	
8a. NAME OF FUNDING / SPONSORING ORGANIZATION U. S. Army Research Office	8b. OFFICE SYMBOL (If applicable)	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER DAAL03-87-C-0031	
8c. ADDRESS (City, State, and ZIP Code) P. O. Box 12211 Research Triangle Park, NC 27709-2211		10. SOURCE OF FUNDING NUMBERS PROGRAM ELEMENT NO. PROJECT NO. TASK NO. WORK UNIT ACCESSION NO.	
11. TITLE (Include Security Classification) Study of SSIN Parallel Processing Interconnection Networks			
12. PERSONAL AUTHOR(S) Dharma P. Agrawal			
13a. TYPE OF REPORT Final	13b. TIME COVERED FROM 10/1/87 TO 9/30/88	14. DATE OF REPORT (Year, Month, Day) October 31, 1988	15. PAGE COUNT 3
16. SUPPLEMENTARY NOTATION The view, opinions and/or findings contained in this report are those of the author(s) and should not be construed as an official Department of the Army position, policy, or decision, unless so designated by other documentation.			
17. COSATI CODES FIELD GROUP SUB-GROUP		18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number) Interconnection Networks, Switches, Parallel Processing Networks	
19. ABSTRACT (Continue on reverse if necessary and identify by block number) <p>The increase in dynamic average path length (DAPL) with network size is moderate while it is significantly less than $\log_2 V$, the number of stages needed in a MIN. The best performance in the case of no fault and single fault, is obtained for the modified Omega and the Zeta SSINs.</p> <p>Keywords include:</p>			
20. DISTRIBUTION / AVAILABILITY OF ABSTRACT <input type="checkbox"/> UNCLASSIFIED/UNLIMITED <input type="checkbox"/> SAME AS RPT. <input type="checkbox"/> DTIC USERS		21. ABSTRACT SECURITY CLASSIFICATION Unclassified	
22a. NAME OF RESPONSIBLE INDIVIDUAL		22b. TELEPHONE (Include Area Code)	22c. OFFICE SYMBOL

Study of SSIN Parallel Processing

Interconnection Networks

Final Report

by

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Date: October 31, 1988

submitted to

U. S. Army Research Office

under contract no. DAAL03-87-C-0031

Accession For	
NTIS GRA&I	<input checked="" type="checkbox"/>
DTIC TAB	<input type="checkbox"/>
Unannounced	<input type="checkbox"/>
Justification	
By	
Distribution/	
Availability Codes	
Dist	Avail and/or Special
A-1	



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Study of SSIN Parallel Processing Interconnection Networks

Problem Studied:

In this work, we consider single stage interconnection networks (SSINs) which have only one stage of switches; in contrast to multistage interconnection networks (MINs), and use recirculation through processors to provide the desired source-destination permutations. The main objective of this work is to obtain an analytical probability model of SSINs and to do simulation for evaluation of the performance of SSINs. We focus our attention on SSINs using 2×2 switches. We have considered four SSINs and simulated different network sizes, loading and routing strategies. The four SSINs are the single stage Omega, the Modified Omega, the Zeta and the ROT networks. In resolving the conflicts, we use two possible cases of processors with and without buffers and three different routing strategies. The strategies are Shortest Remaining Path First, Longest Remaining Path First and Arbitrary Priority. The buffer size is assumed to be large enough to hold any number of requests. For cases without buffers, requests of lower priority are sent to available processors for further routing. The simulation software accepts network type, network size and switch size as inputs and produces the adjacency matrix and distance matrix of the network, the switch dependency graph, the randomly selected permutation samples and their routings, the average dynamic path length, the average conflict number and the maximum path length required to complete a permutation. In general, there is a close agreement between the analytical model and the simulation. Thus the model by itself could be used to study the performance of SSINs. The impact of single stack-at-faults on the dynamic full access capability and the dynamic average path lengths, has also been considered.

Summary of the important results:

The increase in dynamic average path length (DAPL) with network size is moderate while it is significantly less than $\log_2 N$, the number of stages needed in a MIN. The best performance in the case of no fault and single fault, is obtained for the modified Omega and the Zeta SSINs.

List of publications:

1. J. Richard Burke, Chienhua Chen, Tsung-Ying Lee and Dharma P. Agrawal, "*Performance Analysis of Single Stage Interconnection Networks*," accepted for presentation, Taiwan Conference, Dec. 1988.
2. J. Richard Burke, Chienhua Chen and Dharma P. Agrawal, "*Impact of faults on the performance of single stage Interconnection Networks*," under preparation.

Participating Scientific Personnel:

1. Dr. J. Richard Burke: Co-principal Investigator and ARO Staff Research Officer
2. Mr. T. Y. Lee: finished MS degree
3. Mr. Chienhua Chen: currently finishing MS degree